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Section II. REMARKS

The pending claims in the application are 40-45, 47, 49, 51, 61 and 63.

Claim Objections

1. According to the Examiner, claims 40, 61 and 63 recites that the recited top electrode may be formed of Rh or Rh oxide, however, the original disclosure lacks an adequate description regarding this subject matter. Applicants vigorously disagree.

As stated in the MPEP §2163 (I), to satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention at the time of filing. See, e.g., *Vas-Cath, Inc. v. Mahurkar*, 19 U.S.P.Q.2d 1111, 1116 (Fed. Cir. 1991). Furthermore, each claim must be given its broadest reasonable interpretation in light of and consistent with the written description. MPEP §2163 (II)(A)(1) (citing, e.g., *In re Morris*, 44 U.S.P.Q.2d 1023, 1027 (Fed. Cir. 1997)).

Referring to the instant specification, the top electrode "may be formed of a noble metal" (see page 13, lines 11-12; page 14, lines 1-2; and page 14, lines 9-12). It is well known in the chemical arts that noble metals include the metals of Groups VIIB, VIII, and IB of the second and third transition series of the Periodic Table, including Re, Ru, Rh, Pd, Ag, Os, Ir, Pt and Au,¹ said definition being supported by the USPTO when defining the 420/505 patent subclass.²

Thus, giving the claims the broadest reasonable interpretation in light of and consistent with the written description, which is the proper standard, the top electrode comprising Rh or Rh oxide is adequately described in the specification as filed because the specification recites that the top electrode may be formed of a noble metal.

Even if this were not the case, the fact remains that originally filed claim 46 recites that the top electrode comprises a material selected from Rh and Rh oxides. It is well settled in the law that "original claims constitute their own description" and as such, "later added claims of similar scope and wording are described thereby." *In re Koller*, 204 U.S.P.Q. 702, 706 (CCPA 1980) (citing *In re Gardner*, 177 USPQ

¹ See, <http://www.britannica.com/eb/article?tocId=9056014&query=platinum%20group&ct=null>.

² See, <http://www.patentec.com/data/class/defs/420/505.html>.

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396 (CCPA 1973)). Thus, the disclosure adequately describes that the top electrode may be formed of Rh or Rh oxide.

Applicants respectfully request the Examiner withdraw the objection of claims 40, 61, and 63.

2. According to the Examiner, claim 52 recites that oxygen is not incorporated in the electrode material, but the disclosure fails to definitively define whether oxygen is absolutely not incorporated into the electrode material.

Applicants have cancelled claim 52, thereby obviating this objection.

3. Applicants have amended claim 63 according to the Examiner's suggestion to recite "maintained during" in place of "maintained through." Withdrawal of this objection is respectfully requested.

In light of the foregoing discussion and amendments, applicants respectfully request the Examiner withdraw the prior objections to claims 40-45, 47, 49, 51-54, 61 and 63.

Amendment to Claim 40

Claim 40 has been amended herein to recite:

"A microelectronic device structure comprising:

a silicon substrate comprising at least one additional layer selected from the group consisting of a bottom electrode layer, a diffusion barrier layer, an insulating layer and a buffer layer;

a ferroelectric oxide film material positioned over the silicon substrate, wherein the ferroelectric oxide material has a top surface and vicinity thereunder that is substantially stoichiometrically complete in oxygen concentration;

a top electrode comprising a first layer and a second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer of the top electrode comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer of the top electrode is selected from the group consisting of Ir, Rh and mixtures thereof, and wherein the total thickness of the top electrode is in a range

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from about 100 nm to about 500 nm." (emphasis added to show subject matter added to the claim)

Support for this amendment can be found in the instant specification at page 12, lines 13-17 and page 20, lines 10-14.

Claim 40, as amended, is patentable in light of all of the references cited during the prosecution of the presently pending claims.

Rejection of Claims and Traversal Thereof

In the July 14, 2004 Office Action,

claims 40-43, 47, 49, 51-54 and 63 were rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura (U.S. Patent No. 6,229,168); and

claims 44, 45 and 61 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura in view of Miki et al. (WO98/01904 and U.S. Patent No. 6,309,894) and/or Park et al. (U.S. Patent No. 5,892,254).

These rejections are traversed and reconsideration of the patentability of the pending claims is requested in light of the following remarks.

Rejection under 35 U.S.C. §102(e)

In the July 14, 2004 Office Action, claims 40-43, 47, 49, 51, 53 and 63 were rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura (U.S. Patent No. 6,229,168). Applicants traverse such rejection.

It is well established, as a matter of law, that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Further, the elements must be arranged in the prior art reference as required by the claim. See, *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). The Nakamura reference does not meet this standard.

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Claim 40 has been amended to recite:

“A microelectronic device structure comprising:

a silicon substrate comprising at least one additional layer selected from the group consisting of a bottom electrode layer, a diffusion barrier layer, an insulating layer and a buffer layer;

a ferroelectric oxide film material positioned over the silicon substrate, wherein the ferroelectric oxide material has a top surface and vicinity thereunder that is substantially stoichiometrically complete in oxygen concentration;

a top electrode comprising a first layer and a second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer of the top electrode layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer of the top electrode is selected from the group consisting of Ir, Rh and mixtures thereof, and wherein the total thickness of the top electrode is in a range from about 100 nm to about 500 nm.” (emphasis added to show subject matter added to the claim)

Independent claim 63 has been amended correspondingly to claim 40. Thus, both independent claims and all claims depending therefrom now recite that the top electrode, having a thickness from about 100 nm to about 500 nm, is structurally composed of two layers, the first layer is an oxide layer positioned on the ferroelectric material and the second layer is a metal layer positioned on the first layer.

Schematically, the structure recited in claim 40 is equivalent to that shown in FIG. A:

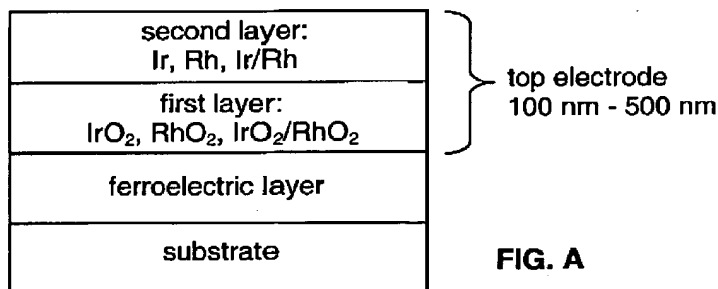
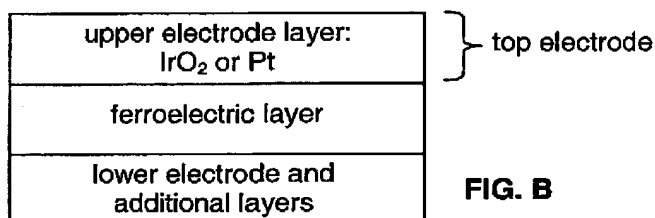


FIG. A

Nakamura relates to ferroelectric capacitors comprising ferroelectric layers and top and bottom electrodes. The relevant teachings of Nakamura are as follows:

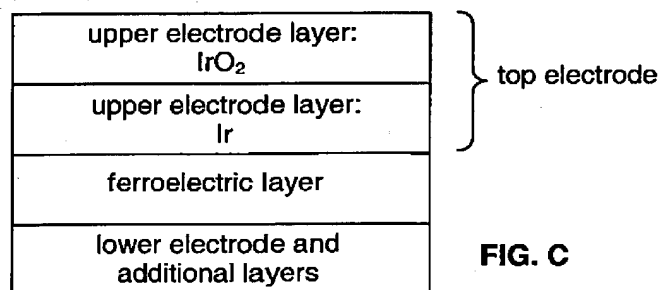
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- (a) Nakamura, at col. 7, lines 3-67 through col. 8, lines 1-31 ("[i]n this embodiment, a silicon oxide layer 4, a lower electrode 13, a ferroelectric layer 8 and an upper electrode 15 are formed on a silicon substrate 2. The . . . upper electrode [is] made of iridium oxide.") describes the structure schematically shown in FIG. B:



As recited in Nakamura, the upper electrode is formed by locating the IrO₂ layer on the ferroelectric layer by *reactive* sputtering (see Nakamura, col. 7, lines 63-65). Clearly there is only a single layer of an oxide or Pt deposited on the ferroelectric layer and certainly no indication that the top electrode comprises two separate layers.

- (b) Nakamura, at col. 9, lines 24-67 through col. 10, lines 1-67 ("In this embodiment, a silicon oxide layer 4, a lower electrode 32, a ferroelectric layer 8 and an upper electrode 35 are formed on a silicon substrate 2. [] [T]he upper electrode 35 is formed by an iridium layer 37 and an iridium oxide layer 33 formed thereon.") describes the structure schematically shown in FIG. C:

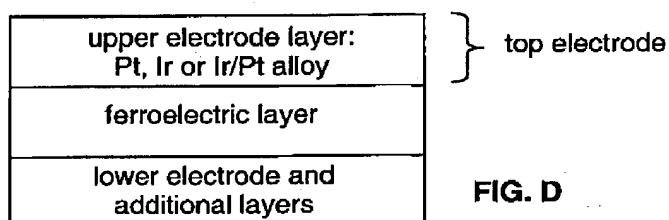


As recited in Nakamura, the iridium layer is deposited by sputtering, i.e., in the absence of oxygen, and the an iridium oxide layer is formed on the surface of the iridium layer by carrying out thermal treatment under an oxygen atmosphere at 800°C for 1 minute (see Nakamura, col. 9, lines 66-67 through col. 10, lines 1-3). In other words, in this Nakamura embodiment, the metal layer is in direct contact with the top surface of the

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ferroelectric layer and then a "cap" of iridium oxide is formed on the top surface of the iridium layer. There is no disclosure, teaching or suggestion to reverse these layers and deposit the oxide directly on the ferroelectric material, as claimed by applicants herein.

- (c) Nakamura, at col. 11, lines 1-67 through col. 12, lines 1-10 ("A platinum layer 112 is formed on the iridium oxide layer 111. [] Then a PZT layer 114 is formed as a ferroelectric material, also a platinum layer 116 is formed thereon as an upper electrode . . . An iridium layer or an alloy layer made of platinum and iridium can be a substitution of the platinum layer 112, 116.") describes the structure schematically shown in FIG. D:



There is no indication in Nakamura how the upper electrode layer of the structure in FIG. D is deposited however, the upper electrode layer of this Nakamura embodiment is not an oxide.

Clearly, Nakamura does not teach or suggest applicants' claimed invention comprising a top electrode having a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof.

The Examiner is respectfully reminded that for a prior art reference to be anticipatory, the elements must be arranged in the prior art reference as required by the claim. *Id.* In other words, the Examiner cannot pick teachings from one embodiment of the prior art reference and arbitrarily combine them with teachings from another embodiment in the same prior art reference, and claim that a *prima facie* case of anticipation has been established.

Likewise, claim 63, which has been amended correspondingly to claim 40 herein, is novel.

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In conclusion, Nakamura does not anticipate applicants' claimed invention. Applicants respectfully request that the rejection under §102(e) of claims 40-43, 47, 49, 51, 53 and 63 over Nakamura be withdrawn.

Moreover, claims 40-43, 47, 49, 51, 53 and 63 are non-obvious in view of Nakamura because Nakamura does not teach or suggest applicants' claimed invention comprising a top electrode having a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof.

Applicants specifically determined that using a two layer top electrode offered many advantages not found in the prior art. As such, applicants developed techniques for depositing the two layer top electrode. For example, the fabrication of the top electrode using different sputtering techniques is discussed in the instant specification at page 12, lines 6-17, as stated below:

"The top electrode may be formed of a metallic (non-oxide) material by sputtering in the presence of oxygen. Such technique may use as the oxygen source pure oxygen, ozone, or an oxygen-containing gas such as N₂O, NO₂, etc. Reactive sputtering with oxygen being present may be employed to deposit an oxide compound, but the sputtering conditions such as pressure, substrate temperature and deposition rate preferably are adjusted to deposit a sub-oxide or pure metal even when oxygen is present.

* * *

Once the ferroelectric or high ϵ film material surface is covered, a different TE formation process can continue, with the oxygen source being turned off, for example."

In other words, the first layer of the top electrode is deposited by a method including *reactive* sputtering (in the presence of oxygen) and the second layer of the top electrode is deposited by sputtering (in the absence of oxygen). The advantages of applicants' claimed invention include, but are not limited to:

"By such technique, the oxygen present in the deposition environment for formation of the electrode material will tend to prevent a net loss of oxygen in the surface of the ferroelectric or high ϵ film material.

* * *

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Sputtered pure metal top electrodes formed in the absence, or non-incorporative presence, of oxygen ("non-incorporative" meaning that such oxygen is not incorporated in the electrode film material despite being present in the film material formation environment) have lower compressive stress characteristics than those sputtered in the presence of oxygen where oxygen is incorporated in the electrode film. Such lower compressive stress electrodes may be desirable to facilitate the subsequent fabrication of additional layers or elements of the overall microelectronic device structure, and/or to enhance the end-use device characteristics of the structure being fabricated. (see instant application, page 12, lines 13-17 and page 13, lines 1-9) (emphasis added)

Thus, applicants' claimed invention includes a top electrode which is capable of preventing a net loss of oxygen from the top surface of the ferroelectric material AND has a lower compressive stress characteristic so as to facilitate fabrication of additional layers thereon. This is accomplished by depositing a first oxide layer, for example IrO₂, directly onto the ferroelectric layer followed by deposition of a second metal layer, for example Ir, directly onto the first layer. Nakamura did not recognize or address the combination of the two foregoing advantages.

As introduced hereinabove, Nakamura does not teach or suggest every limitation of applicants' claimed invention, specifically a top electrode having a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof.

Instead, Nakamura discloses a number of different embodiments with specific focus on the SiO₂-lower electrode region because, as stated in Nakamura, if the ferroelectric layer is formed on a layer, which is not oriented axially, the ferroelectricity of the device is compromised (see Nakamura, col. 1, lines 25-40). Examples of upper electrodes disclosed in Nakamura include (a) a homogeneous Ir layer, (b) a homogeneous IrO₂ layer, or (c) an iridium layer that was thermally treated with oxygen to convert the upper surface of the deposited iridium layer to iridium oxide (in other words, the iridium oxide layer is not in direct contact with the ferroelectric layer, instead the iridium layer is). Furthermore, all of the remnant polarization experiments disclosed in Nakamura disclose the use of a Pt or IrO₂ top electrode only. One skilled in the art reading Nakamura would not readily recognize the importance of the top electrode in the ferroelectric characteristics of the device, much less devise the top electrode layer claimed in applicants' claim 40.

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Moreover, there is no motivation to modify Nakamura to yield applicants' claimed invention. It is well established as a matter of law that the mere fact that references can in some way or ways be modified does not render the resultant modification obvious unless the prior art also suggests the desirability of the modification. See, *In re Mills*, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990).

In the present case, there is no motivation or suggestion in Nakamura to form the microelectronic device structure claimed by applicants herein, specifically a top electrode having a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof. Any suggestion by the Examiner otherwise is hindsight reconstruction, which is legally improper.

In conclusion, Nakamura does not motivate, teach or suggest every limitation of applicants' claimed invention and there is no motivation or suggestion to modify Nakamura. Accordingly, applicants' claims 40-43, 47, 49, 51, 53 and 63 are non-obvious in view of Nakamura.

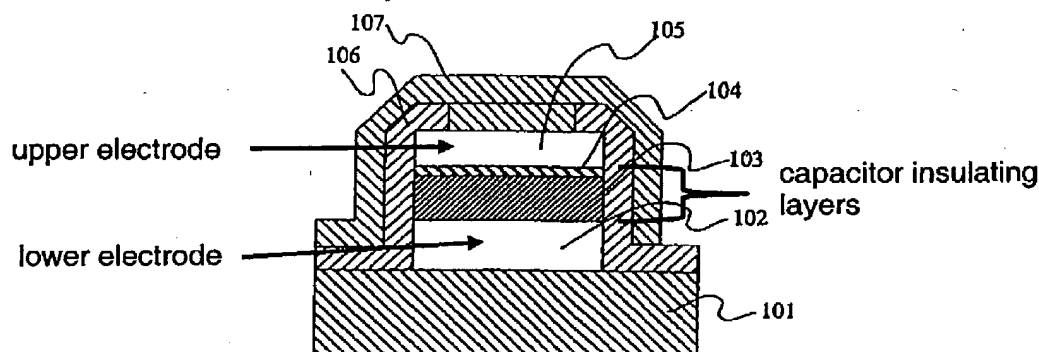
In the July 14, 2004 Office Action, claims 52 and 54 were rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura, or in the alternative, were rejected under 35 U.S.C. §103(a) as being obvious over Nakamura.

Applicants have cancelled claims 52 and 54 thereby obviating this rejection.

In the July 14, 2004 Office Action, 44, 45 and 61 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura in view of Miki et al. (WO98/01904 and U.S. Patent No. 6,309,894) (hereinafter Miki) and/or Park et al. (U.S. Patent No. 5,892,254) (hereinafter Park). Applicants traverse such rejection.

Miki discloses a storage capacitor of a semiconductor memory device (see Miki, Fig. 1, reproduced hereinbelow for ease of reference) having a lower electrode 102, capacitor insulating film 103 (of a high dielectric constant or ferroelectric material), layer 104 with additional oxygen on the surface of the capacitor insulating film 103 and an upper electrode 105 formed on the semiconductor substrate 101.

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Miki Fig. 1

The upper electrode materials disclosed in Miki comprise Pt, Pd, Ni, W, Ti and Mo (see Miki, col. 4, lines 35-37).

According to Miki, degradation and delamination of the capacitor insulating film 103/upper electrode layer 105 interface can be suppressed by forming an additional oxygen layer 104 by annealing the capacitor (generally consisting of 102, 103 and 104) in an oxygen atmosphere after formation of the capacitor, i.e., after the upper electrode is deposited onto the capacitor insulating film 103 but before any subsequent deposition of layers (see Miki, col. 3, lines 1-10 and col. 4, lines 28-33).

Importantly, the additional oxygen layer 104 of the Miki structure is a hyperoxygenated capacitor insulating film layer (see Miki, col. 4, lines 28-33, "The layer 104 with additional oxygen refers to a layer formed when the upper electrode 105 is formed by fully repairing a layer with a minute oxygen vacancy, produced on the surface of the high-dielectric-constant or ferroelectric thin film functioning as the capacitor insulating film 103" (emphasis added) with Miki, col. 2, lines 54-56, "the main cause [of degrading of capacitor characteristics] to be a structural transformation in the vicinity of the boundary between the upper electrode and the high-dielectric-constant or ferroelectric material functioning as the capacitor insulating film, in particular the production of oxygen vacancies on the surface of the metal oxide which is the high-dielectric-constant or ferroelectric material." (emphasis added)).

Inherently, since the oxygen annealing disclosed in Miki occurs after the deposition of the upper electrode, oxygen must be able to pass through the atomic structure of the upper electrode material, e.g., Pt, or else the hyperoxygenated capacitor insulating film layer 104 would not be formed.

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As discussed hereinabove, Nakamura does not motivate, teach or suggest applicants' claimed invention, specifically a top electrode having a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof. Miki does not cure this deficiency.

The additional oxygen layer 104 disclosed in Miki is a hyperoxygenated ferroelectric layer, wherein the oxygen employed during annealing passes through the upper electrode and supplements the crystal structure of the ferroelectric material. In other words, Miki only teaches or suggests a single homogeneous upper electrode layer comprising Pt, Pd, Ni, W, Ti and Mo, not a first top electrode layer and a second top electrode layer, as claimed by applicants herein.

In addition, like Nakamura, Miki fails to recognize the advantages of applicants' claimed invention, including a top electrode which is capable of preventing a net loss of oxygen from the top surface of the ferroelectric material AND has a lower compressive stress characteristic so as to facilitate fabrication of additional layers thereon.

Moreover, if the teachings and methods of Nakamura and Miki were to be combined, as hypothesized by the Examiner, even though as mentioned there is no motivational or logical basis for making such combination, the fact remains that Miki by such modification would be rendered unsatisfactory for its intended purpose, and as such, a *prima facie* case of obviousness has not been established. *See, In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As introduced hereinabove, Miki requires that the upper electrode structure be oxygen permeable so that oxygen can be introduced to the upper electrode/capacitor insulating film interface. If the upper electrode acts as an oxygen barrier in any way, the top surface of the capacitor insulating film will not become hyperoxygenated and as such, the ferroelectrical capabilities of the Miki structure will be compromised.

This is exactly what would happen to the Miki structure if the Miki and Nakamura references were combined, as suggested by the Examiner. The Miki top electrode must be permeable to oxygen while the Nakamura top electrode must be impervious to oxygen. Depositing an oxygen impervious layer atop the capacitor insulating film would ensure that no oxygen passed through the top electrode during the Miki

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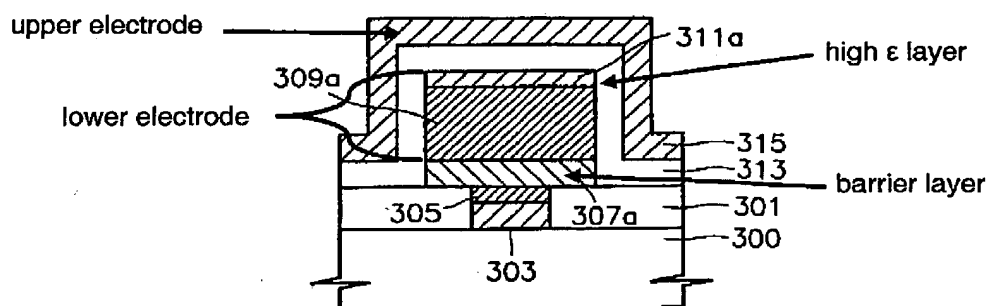
annealing process (when oxygen must pass through the top electrode). Clearly, this would render Miki unsatisfactory for its intended purpose.

Notably, neither reference teaches or suggests which of the distinct top electrode layers, i.e., the permeable versus the impervious, should be used in the Nakamura/Miki combined structure, because there is no motivation, teaching or suggestion to combine the references.

Park teaches an integrated circuit capacitor having a barrier layer between a conductive plug and a lower capacitor electrode. The barrier layer is intended to reduce diffusion of oxygen therethrough and will not be oxidized during a subsequent heat treatment in an oxygen atmosphere. The barrier layer comprises refractory metal, e.g., Ta, Mo and W, and grain boundary filling material, e.g., Ce, Zr, Y, Th, Hf, La, Al and oxides thereof.

Referring to Fig. 3 of Park, reproduced hereinbelow for ease of reference, an insulating layer 301 is formed on a semiconductor substrate 300, and a conductive plug 303 and an ohmic layer 305 are formed in a predetermined region of the insulating layer 301. A stacked structure is formed on the insulating layer 301 and the ohmic layer 305. The stacked structure includes a barrier layer pattern 307a, a first lower electrode pattern 309a and a second lower electrode pattern 311a.

The barrier layer pattern 307a is formed of refractory metal and grain boundary filling material. The first lower electrode pattern 309a is formed of a platinum group metal and the grain boundary filling material, e.g., Ce, Zr, Y, Th, Hf, La, Al and oxides thereof. The second lower electrode pattern 311a is formed of a platinum group metal. A high dielectric constant layer 313 and an upper electrode 315 are also included on the stacked structure.



Park Fig. 3

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In short, like Nakamura, the Park reference is principally focused on the layers between the silicon substrate and the ferroelectric layer (high ϵ layer). The only teachings related to the composition of the upper electrode of Park are that the "upper electrode 315 can be formed of a platinum group metal" (see Park, col. 6, lines 8-9); "[p]latinum is then deposited to form the upper electrode 415" (see Park, col. 7, lines 22-23); and "the upper electrode 415 can be formed of a platinum group metal, such as Pt, Ir or Ru" (see Park, col. 7, lines 24-26).

Like Nakamura and Miki, Park fails to recognize the advantages of applicants' claimed invention, including a top electrode which is capable of preventing a net loss of oxygen from the top surface of the ferroelectric material AND has a lower compressive stress characteristic so as to facilitate fabrication of additional layers thereon.

Clearly, considering the recited teachings of Park, there is no motivation, teaching or suggestion in Park that the top electrode have a first and second layer, wherein the first layer directly contacts the top surface of the ferroelectric oxide film material and the second layer directly contacts the first layer, wherein the first layer comprises a material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof and the second layer is selected from the group consisting of Ir, Rh and mixtures thereof, as claimed by applicants herein. Thus, Park does not cure the deficiencies of Nakamura.

Moreover, the combination of Nakamura, Miki and Park does not motivate, teach or suggest a top electrode having a first oxide layer and second metal layer positioned on the first layer with an overall thickness from about 100 nm to about 500 nm. As clearly stated in the specification, there are definite advantages to this specific thickness because thicknesses less than 0.1 μm have high electrical resistance while thicknesses greater than 0.5 μm incur high fabrication cost and exhibit poor adherence (see instant specification, page 20, lines 10-14). These advantages are not recognized by any of the cited references either alone or in combination.

The Examiner is respectfully reminded that "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984)) (emphasis in original). The examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references" *In re Fritch*, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992) (emphasis added).

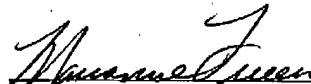
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In conclusion, the combination of Nakamura and Miki and/or Park does not motivate, teach or suggest every limitation of applicants' claimed invention and the combination of Nakamura and Miki would render Miki unsatisfactory for its intended purpose. Accordingly, applicants respectfully request withdrawal of the §103(a) rejection of claims 44, 45 and 61 over Nakamura in view of Miki and/or Park.

CONCLUSION

Applicants have satisfied the requirements for patentability. All pending claims are free of the art and fully comply with the requirements of 35 U.S.C. §112. It therefore is requested that Examiner Hu reconsider the patentability of the pending claims, in light of the distinguishing remarks herein, and withdraw all rejections, thereby placing the application in condition for allowance. Notice of the same is earnestly solicited. In the event that any issues remain, Examiner Hu is requested to contact the undersigned attorney at (919) 419-9350 to resolve same.

Respectfully submitted,



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